

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 0 704 909 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
03.04.1996 Bulletin 1996/14

(51) Int Cl. 6: H01L 29/786, H01L 21/336,
H01L 21/28

(21) Application number: 95306521.6

(22) Date of filing: 15.09.1995

(84) Designated Contracting States:
DE FR GB IT

(72) Inventor: Cunningham, James A.
Saratoga, California 95070 (US)

(30) Priority: 30.09.1994 US 315955

(74) Representative: Palmer, Roger et al
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(71) Applicant: SGS-THOMSON
MICROELECTRONICS, INC.
Carrollton Texas 75006-5039 (US)

(54) MOS-type semiconductor device and method for making the same

(57) A semiconductor device includes an insulating support. A strip of semiconductor material has two ends in contact with the insulating support and a midsection extending between the ends. A dielectric layer encircles the midsection, and a conductive layer encircles the dielectric layer. The conductive layer has a substantially constant width such that a gate electrode formed within the conductive layer is fully self-aligned with drain and source regions formed within the ends.

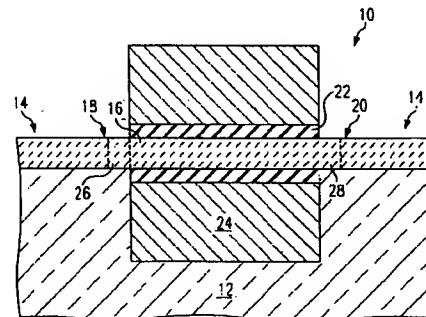


FIG. 1

EP 0 704 909 A2

Description

The present invention relates generally to semiconductor devices and more particularly to a thin-film transistor (TFT).

The concept of placing the conducting channel of an MOS transistor within a thin film of polycrystalline silicon (poly) is quite old dating back to the late 1960s. But despite a significant research and development effort, these devices and their amorphous silicon counterparts enjoyed little commercial success until recent years. This is because, compared to MOS transistors prepared on single crystal substrates, thin film transistors (TFTs) using poly or amorphous materials typically exhibit much lower transconductance due to the lower carrier mobility. They were also often characterized by high and unrepeatable threshold voltages due to charging effects arising from traps believed to reside at the grain boundaries.

In the early 1980s, TFTs prepared with hydrogenated amorphous silicon (α -Si:H) were studied for thin-film image sensor applications. Recrystallization of this or similar material led to relatively high performance poly TFTs. By the late 1980s poly TFTs were applied in production quantities to active-matrix-type liquid crystal displays (LCDs). These products use glass or quartz substrates. The TFTs are relatively large in size compared to conventional MOS transistors and operate at higher voltages than those commonly used in digital applications.

TFTs have not been applied to standard CMOS devices in large production quantities as yet although many papers have been published in recent years on this general topic. Koichiro Ishibashi et al., "A 1V TFT-Load SRAM Using a Two-Step Word-Voltage Method," *IEEE ISSCC*, pg. 206 (1992); Sji Murakami et al., "A 21 mW CMOS SRAM for Battery Operation," [Mitsubishi Electric], *ISSCC*, pg. 46 (1991); Katsuro Sasaki et al., A 7ns 140mW CMOS SRAM with Current Sense Amplifier," [Hitachi], *ISSCC*, pg. 208 (1992); Hiroyuki Goto et al., "A 3.3V 1.2 ns 16Mb CMOS SRAM," [NEC], *ISSCC*, pg. 216 (1992); C.T. Liu et al., "High Reliability and High Performance 0.35 μ m Gate-Inverted TFTs for 16 Mbit SRAM Application Using Self-Aligned LDD Structures," [AT&T], *IEEE IEDM*, pg. 823 (1992); J.P. Colinge et al., "Silicon-on-Insulator Gate-All-Around Device," *IEDM*, pg. 595 (1990); J.D. Hayden et al., "A High-Performance Quadruple Well, Quadruple Poly BiCMOS Process for Fast 16 Mb SRAMs," *IEEE IEDM*, pg. 819 (1992) reported in 1992 an experimental SRAM cell, see Koichiro Ishibashi et al., "A 1V TFT-Load SRAM Using a Two-Step Word-Voltage Method," *IEEE ISSCC*, pg. 206 (1992).

TFTs, although often larger than their single-crystal counterparts, are often used to produce integrated circuits having reduced areas. For example, a TFT may be used as a load device in a static random access memory (SRAM) cell. Typically, a TFT is a field-effect transistor (FET) having its channel, drain, and source regions formed from a strip of semiconductor material that has

been formed on a dielectric substrate, such as quartz or glass. Thus, unlike a conventional FET that is formed in a semiconductor substrate, a TFT may be formed in vertical alignment with a semiconductor structure, such as an SRAM cell. Such stacking of integrated-circuit components often provides a significant reduction in the area of the integrated circuit.

However, TFTs often exhibit significantly lower "on" currents, I_{dsat} , than do their conventional counterparts with similar W/L ratios. Additionally, the switching speed of a TFT is often too slow for certain applications.

A method is disclosed for building poly TFTs with self-aligned gate electrodes which completely encircle the channel region. This encirclement increases the width dimension by a factor of two at a minimum. The increased "on" current flow is greater than this because the conduction is not only along two inverted channels, but through volume inversion as well. Volume inversion effects have been reported for dual-gate devices, that is, MOS transistors with upper and lower gate electrodes. See E. Simoen et al., "A Low-Frequency Noise Study of Gate-All-Around SOI Transistors," *IEEE Tran. on Electron Dev.* 40(11):2014 (1993).

The inventive process involves forming a cavity below a poly film patterned into narrow strips. The poly layer is used to form the channel, and source and drain regions of the TFT. The cavity and a channel or slot are provided into the dielectric substrate using standard photoresist methods and etching techniques. A second film of highly conformal LPCVD poly is then let into the cavity and channel somewhat analogous to the "damascene" process, used for metal layers and reported in recent years by IBM. See, R.R. Uttecht and Robert M. Geffken, "A Four-Level-Metal Fully Planarized Interconnect Technology For Dense High Performance Logic and SRAM Applications," *VMIC*, pg. 20 (1991). The second poly film forms a self-aligned gate electrode around the transistor channel region in the thin first poly film. Functional n- or p-channel transistors are created using only two photomasking steps. The minimum transistor length is 4λ , where λ is the minimum feature size. This compares to standard MOS technology, which provides minimum poly line widths (transistor lengths as viewed from the surface of the wafer) of 2λ .

It is a basic object of the invention to provide a process for improving the on current and performance of poly TFTs such that these devices may be used more broadly in various applications of integrated circuits.

In accordance with the present invention, a semiconductor device, which includes an insulating support, is provided. A strip of semiconductor material has a pair of opposing ends in contact with the insulating support and a midsection extending between the ends. A layer of dielectric material encircles the midsection, and a layer of conductive material encircles the dielectric layer.

In one aspect of the invention, the semiconductor device is a TFT formed on a dielectric substrate. The opposing ends form the source and drain regions respec-

tively, and the midsection forms the channel region. The dielectric layer and the conductive layer form the gate insulator and the gate electrode respectively. In another aspect of the invention, the source and drain regions respectively include lightly doped source and drain regions.

An advantage provided by one aspect of the present invention is an increase in "on" current without an increase in either V_{ds} or V_{gs} .

An advantage provided by another aspect of the present invention is an increase in switching speed.

According to a first aspect of the present invention there is provided a semiconductor device, comprising an insulating support, a strip of semiconductor material having two ends contacting said insulating support and a midsection extending between said ends, a layer of dielectric material encircling said midsection, and a layer of conductive material encircling said dielectric layer and having a substantially constant width.

Said insulating support may comprise a dielectric material. Said semiconductor material may comprise polysilicon. A first of said ends may form a drain region, a second of said ends may form a source region, and said midsection may form a channel region. Said conductive layer may form a gate electrode. Said midsection may be substantially planar with respect of said ends and said insulating support. Said dielectric layer may form a gate insulator.

According to a second aspect of the present invention there is provided a semiconductor device, comprising a body of semiconductor material having a source region, a drain region, and a channel region a gate insulator encircling said channel region, and a gate electrode encircling said gate insulator and completely self-aligned with said source and drain regions.

Said source region and said drain region may each comprise a lightly doped region adjacent to said channel region. Said gate insulator may comprise silicon dioxide. Said gate electrode may comprise polysilicon. Said semiconductor material may comprise polysilicon.

According to a third aspect of the present invention there is provided a semiconductor device comprising first and second doped semiconductor regions spaced from each other, a third doped semiconductor region positioned between said first and second regions, said third region having a lower doping concentration than said first and second regions, an insulator encircling said third region, and a layer of conductive material encircling said insulator and having a substantially constant width.

Said first and second regions may be of a first type of semiconductor material and said third region may be of a second type of semiconductor material. Said first and second regions may include lightly doped regions adjacent said third region.

According to a fourth aspect of the present invention there is provided a method for forming a semiconductor device, comprising forming a strip of semiconductor material on an insulating support, forming a cavity in said

insulating support beneath a midsection of said strip, forming an insulator around said midsection, and forming a self-aligned electrode around said insulator.

Said step of forming a cavity comprises anisotropically etching openings along opposing sides of said midsection, and isotropically etching said openings such that said openings merge to form said cavity.

The method may further comprise doping said midsection to form a channel region and doping ends of said strip adjacent said midsection to form source and drain regions.

The method may further comprise lightly doping portions of said source and drain regions adjacent said channel region to form lightly doped source and drain regions.

According to a fifth aspect of the present invention there is provided a method for forming a transistor, comprising forming a strip of semiconductor material on an insulating support, forming a cavity in said insulating support beneath a midsection of said strip such that ends of said film adjacent said midsection are in contact with said insulating support, forming a gate insulator around said channel, forming a channel of the transistor within said midsection, forming a gate electrode around said gate insulator, and forming drain and source regions of the transistor within respective ones of said ends such that said gate electrode is fully self-aligned with said drain and source regions.

Said step of forming a strip may comprise forming a layer of polysilicon on said insulating support, and etching said layer to form said strip.

Said step of forming a strip may comprise forming a layer of amorphous silicon on said insulating support, etching said layer to form said strip, forming a first dielectric layer over said insulating support and said strip, forming a second dielectric layer over said first dielectric layer, and flowing said first and second dielectric layers to form a planar surface and to convert said amorphous silicon into polysilicon.

Said step of forming said cavity comprises forming on said strip and said insulating support a layer having a substantially planar surface, forming on said layer a mask that exposes said midsection, anisotropically etching said layer and said insulating support to form openings adjacent sides of said midsection, and isotropically etching said insulating support such that said openings merge beneath said midsection to form said cavity.

Said step of forming a gate electrode may comprise filling said cavity with an electrically conductive material.

The method may further comprise lightly doping portions of said drain and source regions adjacent said channel.

Some embodiments of the invention will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1 is a cross-sectional view of a semiconductor structure in accordance with the present invention.

Figure 2 is a cross-sectional view of a strip of semiconductor material formed on the insulating support.

Figure 3 is a cross-sectional view of the structure of Figure 2 with the addition of a planar layer.

Figure 4 is a top view of the structure of Figure 3 with the addition of a mask layer.

Figure 5 is a cross-sectional view taken along lines A-A' of the structure of Figure 4 after it has been anisotropically etched.

Figure 6 is a top view of the structure of Figure 5 after it has been isotropically etched.

Figure 7 is a cross-sectional view of the structure of Figure 6 taken along lines B-B' of Figure 3.

Figure 8 is a cross-sectional view of the structure of Figure 7 after removal of the mask layer and the addition of a gate oxide and an electrically conductive layer.

Figure 9 is a cross-sectional view of the structure of Figure 8 following etching and during a first self-aligned impurity implantation process.

Figure 10 is a view of the structure of Figure 9 during a second self-aligned impurity implantation process.

Figure 11 is a cross-sectional view of the structure of Figure 10 taken along lines B-B' of Figure 3.

Figure 1 is a cross-sectional view of a semiconductor device 10 according to the present invention. Device 10, which is an FET, includes an insulating support 12 and a strip of semiconductor material 14. In one aspect of the invention, insulating support 12 is formed from a dielectric such as SiO_2 or glass over a semiconductor substrate, and strip 14 is formed from polysilicon to form a TFT. Strip 14 includes a channel 16 and source and drain regions 18 and 20. A gate insulator 22 encircles channel 16, and a gate electrode 24 encircles gate insulator 22. Because gate electrode 24 completely encircles channel 16, the on current and transconductance of device 10 is increased approximately 2-5 times greater than the on current and transconductance of a device having a gate electrode along only a top portion of the channel 16 surface. Additionally, device 10 may include lightly doped source and drain regions 26 and 28, which lower the electric field at drain 20 to reduce the tendency of electrons from drain 20 to become lodged in gate insulator 22. Such lodging, commonly referred to as the "hot electron" problem, may over time shift the threshold voltage of device 10. Furthermore, as discussed below, gate electrode 24 is self-aligned to channel 16. Such self-alignment significantly reduces the size of the device and also reduces parasitic capacitances such as the Miller capacitance, and therefore increases the switching speed of device 10.

Figures 2-10, illustrate a method for forming device 10. Referring to Figure 2, strip 14 of semiconductor material, having a width W , is formed on an insulating support 12. In one aspect of the invention, the strip 14 is a layer of amorphous silicon deposited on insulating support 12, which is an SiO_2 layer over a silicon substrate, with a low pressure chemical vapor deposition (LPCVD) process. The thickness of the amorphous silicon film is in the range of approximately 500 - 2500 Å. Typically, the thinner the film, the lower the threshold voltage of the

TFT. The deposition temperature is preferably kept between 475 - 650°C so that few nuclei are present for the subsequent grain growth process. The amorphous silicon may be deposited using a source gas of either SiH_4 , which is the conventional gas used, or Si_2H_6 . Si_2H_6 allows the LPCVD to be performed at approximately 475°C and still produce a film that is acceptable. For some devices, such as liquid crystal displays (LCDs), the insulating support 12 may be glass or quartz. An LPCVD process at such a low temperature (approximately 475°C) allows insulating support 12 to be glass or quartz.

Alternatively, the silicon film 14 may be formed as polysilicon. Typical polysilicon formation temperatures range from 650 - 950°C for forming polysilicon on an SiO_2 layer over a silicon substrate. In one embodiment, this polysilicon film may then be made amorphous by ion implantation of silicon. Typically, an implantation level of about 5×10^{15} atoms/cm² at about 75 KEV is sufficient, although the level may vary depending upon the thickness of the deposited film. The growth conditions, and subsequent implant, if necessary, should be such that the deposited film is made as amorphous as possible. Alternatively, the strip 14 may remain polycrystalline silicon and the inventive device formed from polycrystalline silicon as the channel, source and drain regions 16, 18, and 20.

Next, the amorphous silicon film 14 is exposed to a relatively long, low temperature anneal in N_2 or AR to convert the amorphous silicon to large grained polysilicon. Specifically, this anneal is performed at temperatures approximately in the range of 475 - 600°C and for a time period approximately in the range of 20 - 100 hours. However, the temperature during the annealing process is low enough to prohibit the generation of additional nucleation sites or small crystals, but high enough to allow existing crystallites to grow through solid-state diffusion. Such an annealing process produces a polysilicon film having grain sizes of approximately 5 μm and larger. Alternatively, the amorphous silicon film may be converted to large grain polysilicon by using existing laser recrystallization methods.

The amorphous silicon film is converted into large-grained polysilicon because larger grains produce improved TFTs. For example, the larger grains typically reduce the number of charges that may be stored at carrier traps located mainly at the grain boundaries. Conversely, small grains often generate many such traps, which often force a significant portion of the gate voltage applied to the TFT to be wasted in the work of charging and discharging these trap sites instead of creating an inversion layer, i.e., forming the channel, to turn the TFT on. To further reduce the charge density at the grain boundaries, the polysilicon layer may be passivated with hydrogen (H). Such passivation reduces the threshold voltage and sub threshold leakage currents of the TFT. There are many known ways in which the polysilicon layer may be hydrogen passivated, including a long bake in an appropriate forming gas or H₂ applying plasma-en-

hanced chemical vapor deposition (PECVD) silicon nitride layers, immersing the semiconductor structure 10 in a hydrogen plasma at approximately 300°C, or by high-dose ion implantation with protons.

Alternatively, acceptably large grained polycrystalline silicon may be formed for strip 14, using any suitable technique, including the direct formation of polysilicon on a glass or SiO₂ layer.

Once the polysilicon layer 14 has been formed on insulating support 12, one or more polysilicon strips 14 are formed using existing photolithography methods. In one aspect of the invention, width W is 2λ, where 2λ is the minimum feature-size capability for the width of the polysilicon layer 14 for the process technology being used.

Referring to Figure 3, after the formation of polysilicon strip 14, a planar layer 30 is formed over insulating support 12 and strip 14. In one aspect of the invention, layer 30 includes a layer 32 of silicon dioxide (SiO₂) that is approximately 2,000 Å thick, and a layer 34 of phosphorous glass or boron doped glass that is approximately 5,000 Å thick. Layer 34 is then flowed to give a planar surface 36. In one aspect of the invention, SiO₂ layer 32 is deposited using either a conformal chemical vapor deposition or a low pressure chemical vapor deposition. Next, layer 34 is flowed at an appropriate temperature, typically in the range of 800°-1100°C for some applications, though lower temperatures may be used if desired to give approximately flat upper surface 36. Alternatively, layer 30 having planar surface 36 may be formed from a spin-on glass film using existing techniques. This is useful for LCDs formed on glass or quartz.

Referring to Figure 4, which is a top view of the structure of Figure 3, a photoresist mask 38 is formed on surface 36 and etched to expose midsection 16, which has a length L. In one embodiment of the invention, length L is approximately equal to width W. The exposed portions of layer 30 and insulating support 12 are anisotropically etched to give a structure having the view shown in Figure 5 taken along lines A-A of Figure 4. An anisotropic etch process having a high SiO₂/Si selectivity is preferred. Such an anisotropic etch may be performed using existing ion-assisted plasma etch processes that use various fluorocarbon plasma chemistries. As shown in Figure 5, the anisotropic etch completely removes the exposed portion of layer 30 and etches into insulating support 12 a depth of approximately λ, which is about W/2, below the bottom of the midsection 16. Thus, this anisotropic etch forms on either side of strip 14, at the midsection 16, open regions 42.

Referring to Figure 6, the exposed portions of insulating support 12 and layer 30 are then isotropically etched to give an undercut whose boundary is shown by dotted line 40. The amount of undercut within regions 42 is such that an intermediate cavity 46 (Figure 7), which is beneath midsection 16, is formed because the insulating layer 12 is etched through under the midsection 16. Such an isotropic etch may be performed using an

aqueous solution of HF, such as buffered oxide etch (BOE), to a desired depth. In one embodiment, a depth approximately W/2 beyond the original depth of openings 42 after the anisotropic etch is appropriate. However, a smaller undercut is desired in some designs and, for a large gate electrode, a larger undercut is desired, as much as 2λ or greater.

Referring to Figure 7, which is a cross-sectional view taken along lines B-B of Figure 6, one can see that cavity 46 is formed beneath midsection 16 of strip 14. The dotted line shows the depth of openings 42 and the solid line the cavity 46 after the isotropic etch.

Referring to Figure 8, a gate insulator or dielectric 48 is formed such that it completely encircles midsection 16 of strip 14. Because the length of midsection 16 is defined by the width of cavity 46, the gate electrode will be self-aligned with midsection 16, which will become the channel region of the TFT. Such self-alignment will reduce the Miller parasitic capacitance, which can be increased if the gate electrode overlaps the source or drain regions 18 and 20 (Figure 1). The thickness of gate insulator 48 may vary within the range of approximately 150 - 500 Å, depending upon the desired threshold voltage. Gate insulator 48 may be formed using a combination of thermal oxidation followed by conformal CVD of tetra-ethyl-ortho-silicate (TEOS)-based silicon dioxide. Alternatively, gate insulator 48 may be grown thermally in dry oxygen (O₂). Or, gate insulator 48 may be formed using only CVD as is used to form existing TFTs, or using a chemical-vapor deposited silicon-nitride-gate dielectric process. In one aspect of the invention, before gate insulator 48 is formed, the exposed midsection 16 can be thinned by light oxidation and a BOE etching if desired to form a specific-size device.

Next, midsection 16 is implanted with a suitable dopant to form the channel of the TFT. For example, to form an N-channel transistor, midsection 16 may be implanted with boron, in the range of approximately 10¹² atoms/cm². Alternatively, to form a P-channel device, channel region 16 may be left undoped, though typically the channel 16 is lightly implanted with arsenic (As), to have the desired threshold characteristics selected by the designer using known design tools. Mask layer 38 is removed either before or after midsection 16 is implanted to form the channel 16.

Still referring to Figure 8, structure 10 is then coated with a layer 50 of polysilicon. As shown, layer 50 completely fills in openings 42 and cavity 46, to completely encircle both gate oxide 48 and channel 16. Depending upon the deposition process used, some voids 52 may exist in the portion of polysilicon layer 50 in the cavity 46 beneath channel 16. However, it is believed that such voids have no adverse effect on the performance of the resulting TFT, and may be avoided altogether in some polysilicon deposition techniques.

After it has been deposited, polysilicon layer 50 is doped and etched to the surface of glass layer 30. In one aspect of the invention, polysilicon layer 50 is first doped

with an N⁺ implant or diffusion. The top portion of layer 50 may be removed with existing processes, such as chemical mechanical polishing (CMP), or if photoresist mask 38 has small enough openings, an anisotropic plasma etch may be used to remove the poly layer 50. The plasma chemistry should have a high selectivity of Si to SiO₂ such as that found in SF₆-based ion-assisted plasma etching. Alternatively, the top portion of layer 50 may be etched first, and the portion of layer 50 remaining in cavity 46 and openings 42, i.e., the portion of layer 50 that forms gate electrode 24, may be doped afterwards. Depending upon the doping process used, the upper portion 54 of gate electrode 24 may be more highly doped than the lower portion.

Referring to Figure 9, at this point in the process, layer 30 may be removed, and the end portions of strip 14 adjacent to channel 16 may be suitably doped to form source and drain regions 18 and 20 (Figure 1) of the TFT. The doping of the source and drain regions 18 and 20 also implants dopant into the top and exposed sidewall portions of the gate electrode 24. A later diffusing step will drive the dopant under the channel 16, into lower portions 54 to ensure that it is doped, if it has not already been doped in a previous step. The source and drain regions 18 and 20 are thus also formed as self-aligned with the gate electrode 24.

The layer 30 is etched back using an appropriate masking scheme to form spacers 56. In one aspect of the invention, the width S of spacers 56 is approximately 0.5 μm. As is known in the prior art, where S equals approximately 0.15 μm, the on/off current ratio for the resulting TFT is approximately 10⁴ as compared to 10² for non-LDD devices. Furthermore, the on/off current ratio where S equals approximately 0.45 μm is approximately 10⁷. Following the formation of spacers 56, strip 14 is implanted with a dopant. For example, in one aspect of the invention, layer 14 is doped with As using an implant level of approximately 10¹⁵ atom/cm² to form N⁺ source and drain regions 18 and 20, which in Figure 9 would begin at the outer edges of spacers 56.

Referring to Figure 10, spacers 56 may then be removed such as with a BOE or plasma etching. Next, a light dose of dopant is implanted to form lightly-doped regions 26 and 28 of an LDD-type structure. The LDD structure is thus self-aligned with the gate electrode and channel region using side wall oxide spacers, providing significant size and device operation features not previously possible in polysilicon devices formed over an insulating substrate. For example, to produce regions 26 and 28 of an N⁻ material, a light dose of a value appropriate for LDD devices of As is implanted through an applied oxide layer 58. The structure 10 may then be lightly oxidized to heal any edge voids in the gate dielectric 48. The dopants may then be activated by using rapid thermal annealing (RTA) to reduce lateral diffusion.

In an alternative embodiment of the invention, after the glass layer 30 is removed, and an implant oxide is formed over strip 14 and gate electrode 24, a light dopant

implant may be performed to form drain regions 18 and 20 from a lightly doped material. Next, spacers 56 are formed and a second implant is performed such that regions 26 and 28 beneath spacer 16 remain lightly doped and the remaining portions of source and drain 18 and 20 become highly doped to give a resulting TFT with lightly doped drain and source regions 26 and 28.

Figure 11 shows a cross-sectional view of the completed TFT as viewed along lines AA of Figure 4. As will be appreciated, the appropriate electrical interconnections to the source and drain regions 18 and 20 are made using vias, contacts, or the like so that the polysilicon transistor 10 can become an element of a larger circuit. The contacts can be from a lower layer to a device 10 or from a higher layer. Most likely, the electrical interconnections will contact source/drain regions 18 and 20 to respective conductors in the circuit, and the gate electrode 24 to another conductor to provide transistor operations, diode connections, load connections, or the like, as required for each circuit design. The standard techniques known in the art today for forming electrical contacts to poly one, poly two, and other layers, may be used.

It will be appreciated that, although a specific embodiment of the invention has been described herein for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

Claims

1. A semiconductor device, comprising:
an insulating support;
a strip of semiconductor material having two ends contacting said insulating support and a midsection extending between said ends;
a layer of dielectric material encircling said midsection; and
a layer of conductive material encircling said dielectric layer end having a substantially constant width.
2. The device of claim 1 wherein a first of said ends forms a drain region, a second of said ends forms a source region, and said midsection forms a channel region.
3. The device of claim 1 or claim 2 wherein said midsection is substantially planar with respect of said ends and said insulating support.
4. A semiconductor device, comprising:
a body of semiconductor material having a source region, a drain region, and a channel

- region;
- a gate insulator encircling said channel region; and
- a gate electrode encircling said gate insulator and completely self-aligned with said source and drain regions.
5. The device of claim 4 wherein said source region and said drain region each comprise a lightly doped region adjacent to said channel region.
6. A semiconductor device comprising:
- first and second doped semiconductor regions spaced from each other;
- a third doped semiconductor region positioned between said first and second regions, said third region having a lower doping concentration than said first and second regions;
- an insulator encircling said third region; and
- a layer of conductive material encircling said insulator and having a substantially constant width.
7. The device of claim 6 wherein said first and second regions are of a first type of semiconductor material and wherein said third region is of a second type of semiconductor material.
8. The device of claim 6 or claim 7 wherein said first and second regions include lightly doped regions adjacent said third region.
9. A method for forming a semiconductor device, comprising:
- forming a strip of semiconductor material on an insulating support;
- forming a cavity in said insulating support beneath a midsection of said strip;
- forming an insulator around said midsection; and
- forming a self-aligned electrode around said insulator.
10. The method of claim 9 wherein said step of forming a cavity comprises:
- anisotropically etching openings along opposing sides of said midsection; and
- isotropically etching said openings such that said openings merge to form said cavity.
11. The method of claim 9 or claim 10, further comprising doping said midsection to form a channel region and doping ends of said strip adjacent said midsection to form source and drain regions.
12. A method for forming a transistor, comprising:
- forming a strip of semiconductor material on an insulating support;
- forming a cavity in said insulating support beneath a midsection of said strip such that ends of said film adjacent said midsection are in contact with said insulating support;
- forming a gate insulator around said channel;
- forming a channel of the transistor within said midsection;
- forming a gate electrode around said gate insulator; and
- forming drain and source regions of the transistor within respective ones of said ends such that said gate electrode is fully self-aligned with said drain and source regions.
13. The method of claim 12 wherein said step of forming a strip comprises:
- forming a layer of polysilicon on said insulating support; and
- etching said layer to form said strip.
14. The method of claim 12 wherein said step of forming a strip comprises:
- forming a layer of amorphous silicon on said insulating support;
- etching said layer to form said strip;
- forming a first dielectric layer over said insulating support and said strip;
- forming a second dielectric layer over said first dielectric layer; and
- flowing said first and second dielectric layers to form a planar surface and to convert said amorphous silicon into polysilicon.
15. The method of claim 12 wherein said step of forming said cavity comprises:
- forming on said strip and said insulating support a layer having a substantially planar surface;
- forming on said layer a mask that exposes said midsection;
- anisotropically etching said layer and said insulating support to form openings adjacent sides of said midsection; and
- isotropically etching said insulating support such that said openings merge beneath said midsection to form said cavity.

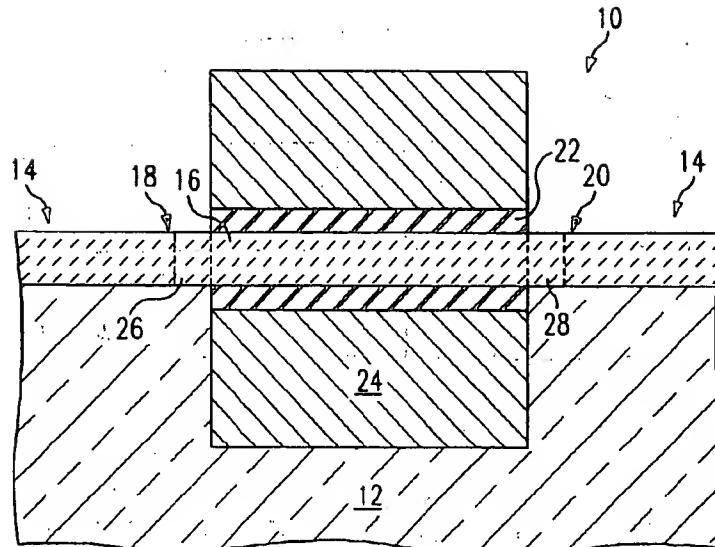


FIG. 1

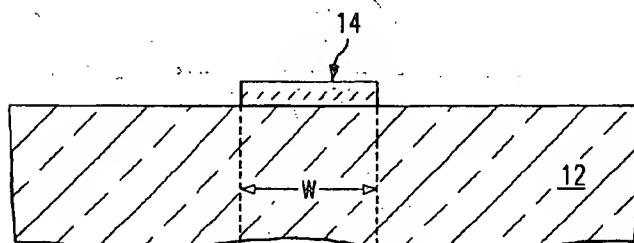


FIG. 2

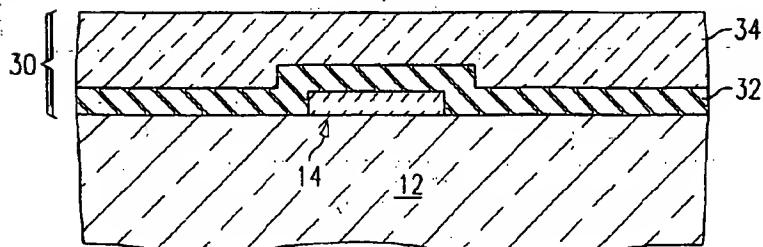


FIG. 3

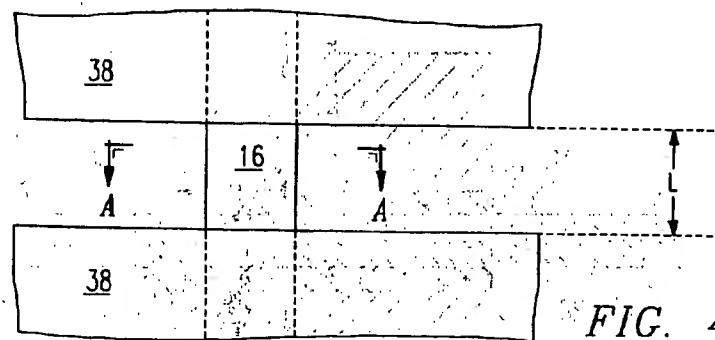


FIG. 4

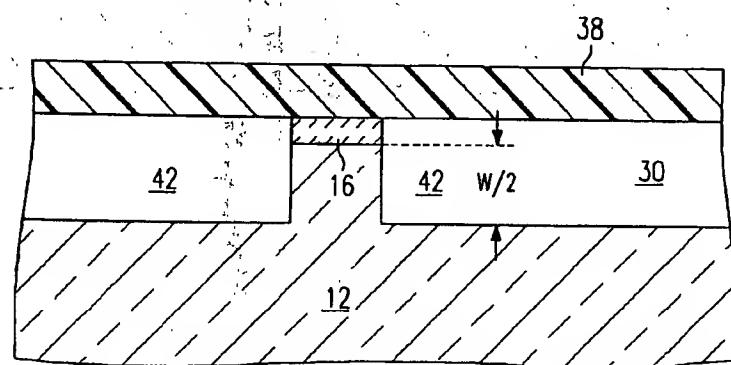


FIG. 5

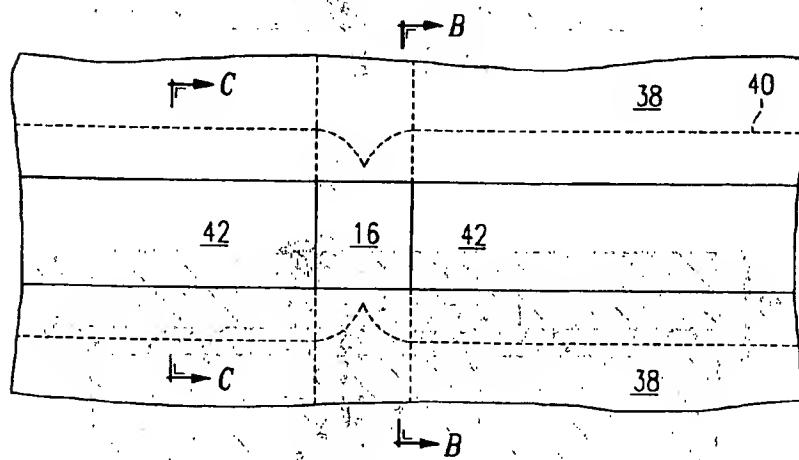


FIG. 6

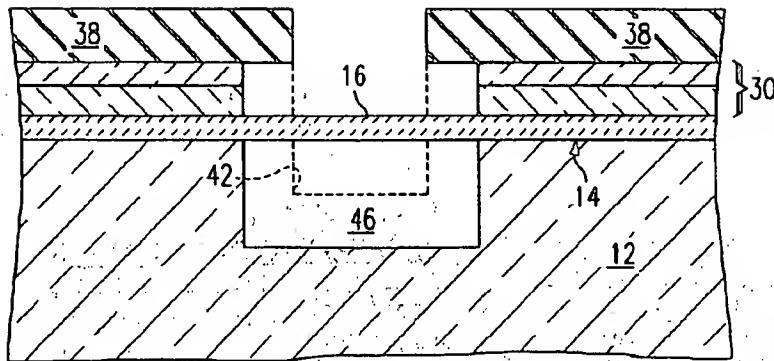


FIG. 7

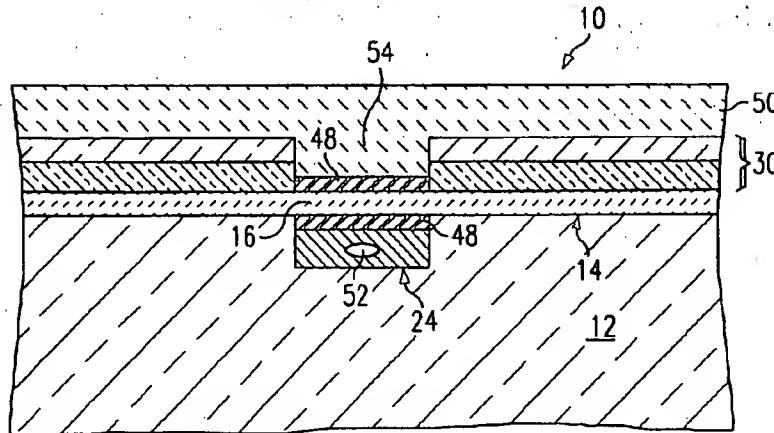


FIG. 8

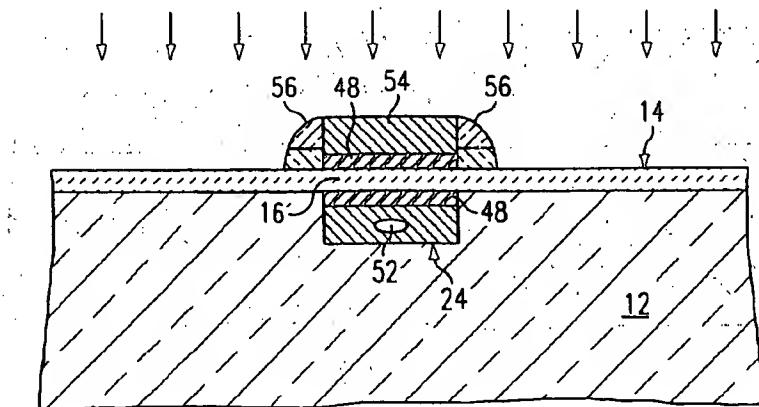


FIG. 9

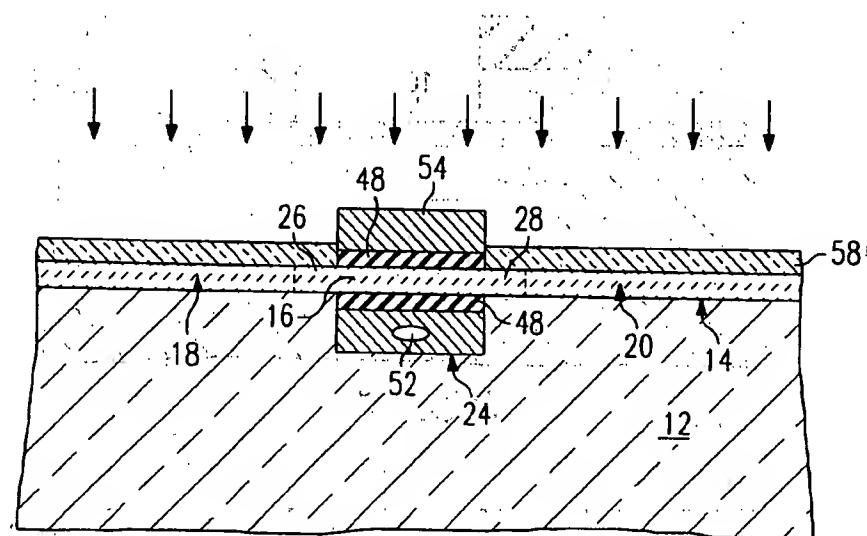


FIG. 10

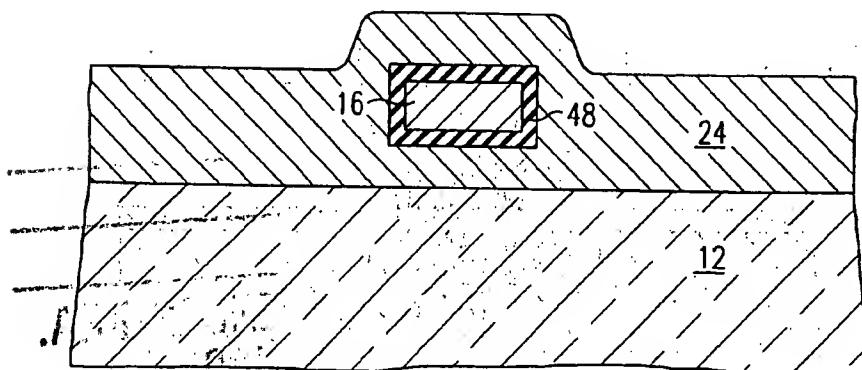


FIG. 11
0011-023 (11)

GET NO:
AL MC
LIC
77

1940-1941. The first year of the new school was opened with a great deal of difficulty.

19. *Leucosia* *leucostoma* *Thunberg* 1784.

the first time, and the author's name is given as "John Smith". The book is described as being bound in red leather with gold tooling, and it is noted that the title page is slightly faded.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
709
710
711
712
713
714
715
716
717
718
719
719
720
721
722
723
724
725
726
727
728
729
729
730
731
732
733
734
735
736
737
738
739
739
740
741
742
743
744
745
746
747
748
749
749
750
751
752
753
754
755
756
757
758
759
759
760
761
762
763
764
765
766
767
768
769
769
770
771
772
773
774
775
776
777
778
779
779
780
781
782
783
784
785
786
787
788
789
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
809
810
811
812
813
814
815
816
817
818
819
819
820
821
822
823
824
825
826
827
828
829
829
830
831
832
833
834
835
836
837
838
839
839
840
841
842
843
844
845
846
847
848
849
849
850
851
852
853
854
855
856
857
858
859
859
860
861
862
863
864
865
866
867
868
869
869
870
871
872
873
874
875
876
877
878
879
879
880
881
882
883
884
885
886
887
888
889
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
909
910
911
912
913
914
915
916
917
918
919
919
920
921
922
923
924
925
926
927
928
929
929
930
931
932
933
934
935
936
937
938
939
939
940
941
942
943
944
945
946
947
948
949
949
950
951
952
953
954
955
956
957
958
959
959
960
961
962
963
964
965
966
967
968
969
969
970
971
972
973
974
975
976
977
978
979
979
980
981
982
983
984
985
986
987
988
989
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2119
212

DOCKET NO: L&L-10178
SERIAL NO: 09/996,279
APPLICANT: Risch et al.
LERNER AND GREENBERG P.A.
P.O. BOX 2480
HOLLYWOOD, FLORIDA 33022
TEL. (954) 925-1100